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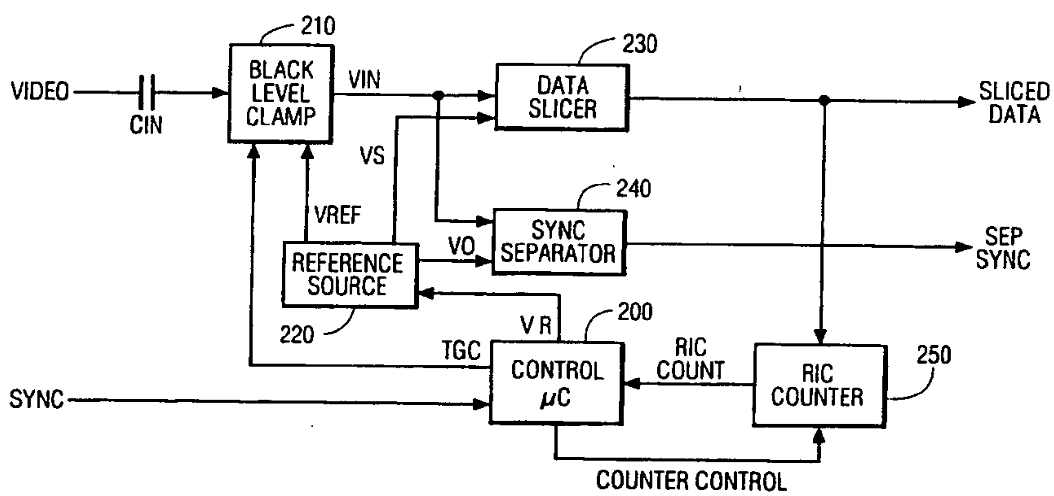

(57) Abstract

An auxiliary video information decoder for extracting an auxiliary video information signal from a video signal includes a data slicer (230) and apparatus (220) for adjusting the slicing level of the data slicer (230). The slicing level is adjusted rapidly until a reference component of the auxiliary information signal is detected during a display interval of the video signal in which auxiliary video information is expected to occur. A count is incremented after display intervals in which the reference component is detected and is decremented after display intervals in which the reference component is not detected. Slicing level adjustment ceases while the count is at least a predetermined number. The apparatus rapidly adapts the slicing level to long-term video signal amplitude changes of significant magnitude (e.g. following a channel change) and maintains a constant slicing level when transient variations occur in the video signal amplitude.

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BIAS CONTROL APPARATUS FOR A DATA SLICER IN AN AUXILIARY VIDEO INFORMATION DECODER

The present invention relates to detection of information that may be present in a video signal during vertical blanking intervals. A video signal typically includes vertical display intervals, or fields, having a plurality of horizontal line intervals, e.g. 262.5 lines per field in NTSC video systems. The beginning of each vertical and horizontal interval is identified by respective vertical and horizontal sync pulses that are included in a composite video signal. During a portion of each vertical interval, information in the video signal may not be intended for display. For example, a vertical blanking interval spans approximately the first 20 horizontal line intervals in each field. In addition, several line intervals adjacent to the vertical blanking period, e.g. line 21, may be within an overscan region of a video display and will not be visible.

The lack of displayed image information during blanking and overscan intervals makes it possible to insert an auxiliary information component, e.g. teletext or closed caption data, into these intervals. Standards such as Federal Communications Commissions (FCC) Regulations define the format for each type of auxiliary information including the positioning of the information within a vertical interval. For example, the present closed captioning standard (see e.g. 47 CFR §§ 15.119 and 73.682) specifies that digital data corresponding to ASCII characters for closed captioning must be in line 21 of field 1. Future modifications to the standard may permit auxiliary information such as closed caption data to be located in other lines, e.g. line 21 of every field.

Auxiliary video information is extracted from the video signal using a decoder. An important part of a decoder is the data

slicer. The data slicer may be a voltage comparator having a video signal carrying auxiliary video information applied to one input. For optimum performance, a reference or "slicing" voltage at a second input of the comparator should be at the midpoint of the peak to peak excursion of the auxiliary video information signal. The output of the comparator would then provide a binary signal representative of the auxiliary information contained in the video signal.

A constant slicing level may not be adequate for all video signals. Video signal levels may vary depending on the source of the video signal. Utilizing a constant slicing level with varying video signal levels may bias the extracted data undesirably toward logic 0 or logic 1 resulting in erroneous data extraction. For example, if the video signal range is 0 IRE to 20 IRE, a slicing level of 10 IRE is desirable while for a video signal range of 0 IRE to 50 IRE, a slicing level of 25 IRE is desirable. If 25 IRE were used as a slicing level for a signal range of 0 IRE to 20 IRE, a logic 1 would never be extracted because the signal never exceeds the slicing level. Thus, it is desirable to adapt the slicing level to the amplitude of the input video signal.

The format of an auxiliary information component such as closed caption data includes provisions to facilitate an adaptive slicing level function. As specified in the FCC standards, a closed caption signal in line 21 begins after the "back porch" interval of the video signal with a 7 cycle burst of a sinusoidal reference waveform designated the "run-in clock" (RIC). The RIC reference component of the auxiliary video data signal is followed in the latter half of the line 21 interval by a data signal component that represents the actual closed caption data. The closed caption data standard establishes that the amplitude of the RIC signal is identical to the amplitude of the data signal. Thus, the average of the RIC signal amplitude is an appropriate slicing level for the subsequent data signal.

One method for developing the slicing voltage is to integrate the sinusoidal RIC signal and use the resulting DC voltage as the bias for the data slicer. A large integrator capacitor may be required to prevent the slicing voltage from changing due to leakage currents discharging the capacitor during the interval between occurrences of auxiliary video data (e.g. the interval from one line 21 to the next for closed caption data). A large capacitor, however, requires long integration intervals to respond to changes in video signal levels when changing the slicing level. For example, in a closed caption signal, the RIC signal is present only for 14 μs (7 cycles of 500KHz sinewave) at 33.3 ms intervals (period of one frame of video). A large capacitor may require a response time on the order of one second to respond to sudden changes in the signal level. A significant amount of auxiliary video information during the response interval may be undetected.

It may be desirable to include an auxiliary video information decoder in a video signal processing integrated circuit (IC). A large integrating capacitor may, however, be too large to be included in the IC. An extra IC pin would be required for connecting an external integrating capacitor.

Although it may be possible to design a fast integrator with component values that are small enough to be included in an IC, the resulting design may exhibit tight tolerances which may be impractical for an integrated circuit design. More specifically, IC parameters may vary during production. A design having tight tolerances may be incompatible (produce unexpected or undesirable performance) as a result of parameter variations during IC production.

The present invention resides, in part, in recognition of the described problems and, in part, in providing an auxiliary video information decoder that solves the problem. In accordance with an aspect of the invention, an auxiliary information decoder

includes a data slicer and means for adjusting the slicing level bias of the data slicer. The slicing level adjustment means comprises means for detecting a reference component of the auxiliary information signal and means for producing a count of the number of times that the reference component is detected. The slicing level is adjusted until the reference component is detected. The count is incremented after display intervals in which the reference component is detected and is decremented after display intervals in which the reference component is not detected. Slicing level adjustment ceases while the count is at least a predetermined number.

The invention may be better understood by referring to the drawing in which:

Figure 1 shows an example of an auxiliary video information signal waveform;

Figure 2 shows in block diagram form a portion of a video signal processing system including auxiliary video signal extraction apparatus according to the present invention;

Figures 3 and 4 show, partially in schematic diagram form and partially in in block diagram form, embodiments of features that are shown in block diagram form in Figure 2;

Figures 5 and 6 show video signal waveforms useful for understanding the operation of the apparatus shown in Figures 2, 3, and 4;

Figures 7 and 9 are flowcharts illustrating alternative operating modes of the apparatus shown in Figures 2, 3, and 4;

Figures 8 and 10 are program listings corresponding to the flowcharts in Figures 6 and 8, respectively;

Figure 11 shows a block diagram of an alternative embodiment of auxiliary video signal extraction apparatus according to the present invention; and

Figures 12A and 12B show, in circuit diagram form, exemplary embodiments of filter functions that are depicted in block diagram form in Figure 11.

An exemplary embodiment of the invention shown in the drawing is described below in detail in the context of closed caption data that complies with the FCC standard closed caption signal depicted in Figure 1. As discussed further below, the invention may also be applicable to the extraction of other forms of auxiliary video data such as teletext.

The portion of a video signal processing system that is illustrated in Figure 2 will be described briefly followed by an in-depth discussion. In Figure 2, coupling capacitor CIN couples input video signal VIDEO to black level clamp 210. A typical value for capacitor CIN is 1 μF. Black level clamp 210 is enabled to clamp the level of signal VIN to a level related to desired black level reference level VREF during intervals determined by control signal TGC from control μC 200, e.g Motorola MC68HC05. The operation of black level clamp 210 is described further below. Signal VIN at the output of black level clamp 210 is coupled to data slicer 230 and sync separator 240 which produce output signals SLICED DATA and SEP SYNC, respectively, by comparing signal VIN to respective reference voltage levels VS and V0.

Signal SLICED DATA is a binary representation of the information in signal VIN. Signal SEP SYNC is a synchronizing waveform having pulses corresponding to the synchronizing pulses in signal VIN. Because signal SEP SYNC is derived from the actual video signal, the sync pulses in signal SEP SYNC provide an accurate indication of when intervals of interest in the video signal, e.g. line 21, actually occur. Signal SEP SYNC may be used by circuits not shown in Figure 2 that capture the binary auxiliary video information on signal SLICED DATA. For example, signal SEP SYNC may be used to generate an enable signal to enable data capture circuitry when binary values representative of auxiliary

video information are occurring on signal SLICED DATA. As an example, the derived enable signal might enable a shift register to begin shifting in (capturing) data values on signal SLICED DATA.

Reference levels VREF, VS, and V0 are generated by reference source 220. Signal VR from control μC 200 is an input to reference source 220 that controls the value of reference level VS. As is described further below, the capability to vary reference level VS permits adapting the slicing level to the amplitude characteristics of video signal VIDEO.

In the embodiment illustrated in Figure 2, adapting the slicing level also involves counter 250. Counter 250 is enabled to count pulses that occur on signal SLICED DATA during intervals defined by one or more control signals from control μC 200 that are labeled COUNTER CONTROL in Figure 2. The counting intervals are established by control μC 200 to coincide with the intervals when the reference component (e.g. run-in clock or RIC) of an auxiliary video information signal is expected to occur. The count value is tested after the RIC interval ends. A count value equal to an expected value indicates that the expected number of RIC pulses have been detected demonstrating that the present slicing level is appropriate for extracting auxiliary video information. If the count value does not equal the expected value, the slicing level is adjusted by modifying the value of signal VS.

As an example of the described operation, control μC 200 monitors signal SYNC to determine when line 21 of field 1 occurs by counting line synchronizing pulses on signal sync. After a delay (e.g. either a software delay routine or a hardware delay) from the beginning of line 21, control μC 200 enables counter 250. The delay value is selected to be within the RIC interval. Counting is then enabled for a period that approximately spans an integral number of cycles of the RIC signal. If the slicing level is properly adjusted, the count value should equal the number of peaks of the RIC waveform that occur during the counting interval. Based on

the timing shown in Figure 1, a delay value of 12 μs and a counting interval of 8 μs should produce a count of 4 if the slicing level is adjusted properly (four cycles of the 500 kHz RIC waveform occur during an 8 μs counting interval).

The above described features are illustrated in more detail in Figures 3 to 6. Figure 3 shows an exemplary embodiment of black level clamp 210, reference source 220, data slicer 230, and sync separator 240 in Figure 2. Figure 4 shows an exemplary embodiment of run-in-clock (RIC) counter 250 in Figure 2. Reference numerals that are the same in Figures 2 and 3, and that are the same in Figures 2 and 4 indicate corresponding features.

In Figure 3, black level clamp 210 includes transmission gate (TG) 302, NOR gate 304, comparator 306, and resistors R1 and R2. Reference source 220 includes 4-to-1 MUX 360 and resistors R3 through R9. Comparators 230 and 240 are embodiments of data slicer 230 and sync separator 240, respectively.

In regard to black level clamp 210, the output of NOR gate 304 controls TG 302 such that TG 302 conducts coupling source VCC to resistor R1 when the output of NOR gate 304 is at logic 1. A logic 0 level at the output of NOR gate 304 causes TG 302 to become non-conductive decoupling source VCC from resistor R1. Typically, TG 302 is produced using MOSFET transistors. As a result, when TG 302 is conductive, it exhibits a characteristic resistance associated with the source-to-drain path through the MOSFET transistors. The value of the resistance depends on design parameters (e.g. transistor width) of the MOSFET transistors.

NOR gate 304 produces a logic 1 output causing TG 302 to conduct as long as control signal TGC from control μC 200 is at logic 0 and the output of comparator 306 is at logic 0. Comparator 306 compares the value of signal VIN to reference level VREF. Values of signal VIN that exceed reference level VREF cause the output of comparator 306 to go to logic 1, thereby causing TG 302

to be nonconductive. When conducting, TG 302 and resistor R1 exhibit a predetermined resistance ratio with respect to resistor R2 of 11:100 as shown in Figure 3. The junction of resistors R1 and R2 is coupled to signal VIN creating a feedback loop.

Assuming signal TGC is at logic 0, the feedback loop and the resistor ratio operate in response to the video signal levels during the sync and blanking intervals in a horizontal line period to charge and discharge node VIN, thereby establishing the desired black level on signal VIN. More specifically, when TG 302 is disabled (non-conductive), the DC level at node VIN discharges via resistor R2. When TG 302 is enabled (conductive), node VIN charges via TG 302 and resistor R1 while discharging via resistor R2. The resistor ratio established by TG 302 and resistors R1 and R2 produces a charge rate that exceeds the discharge rate resulting in a net charging current to node VIN.

To better understand the operation of black level clamp 210, assume that node VIN is initially discharged to 0 volts. In this condition, the level of signal VIN during both sync and blanking intervals of a video line will be less than reference level VREF. Thus, a logic 0 is produced at the output of comparator 306, enabling TG 302 and causing node VIN to charge during both the sync and blanking periods. After a plurality of line intervals, the net charging current will have increased the DC level on node VIN until the level at node VIN exceeds reference level VREF during the blanking interval and is less than reference level VREF during the sync interval. As a result, during the blanking interval the output of comparator 306 will be at logic 1 which disables TG 302 and causes node VIN to discharge. During the sync interval, the level at node VIN during the sync interval is less than level VREF causing node VIN to charge.

The resistance values of the charge path (resistance of TG 302 plus resistor R1) and the discharge path (resistor R2) are selected such that discharge during the sync interval equals

charge during the blanking period when the DC level at node VIN is approximately equal to level VREF. The resulting equilibrium condition clamps the DC level at node VIN to level VREF.

The described operation is based on a resistance ratio between the discharge-path and the charge-path that is determined for the sync and blanking intervals associated with a particular video signal specification. The resistance ratio of 100R (discharge) to 11R (charge) that is shown in Figure 3 is suitable for NTSC standard signals. Other signal standards would require different ratios.

Establishing a clamping function based on resistor ratios is particularly desirable if clamp 210 is included in an integrated circuit (IC). Parameter variations during IC production cause significant variations in specific resistor values. Resistor ratios, however, may be controlled to tight tolerances. Also, it should be noted that approaches to implementing black level clamp 210 other than that shown in Figure 3 may be used.

As described, clamp 210 establishes a desired black level based on sync and blanking intervals having specific durations during each line interval. During the vertical interval, the sync and blanking intervals do not have fixed durations (e.g. wide vertical pulses and narrow equalizing pulses). If clamp 210 operated during the vertical interval, the varying pulse characteristics would cause clamp 210 to undesirably alter the black reference level on node VIN. To prevent the black level from changing significantly, control μC 200 sets signal TGC to logic 1 during the vertical interval disabling the feedback path of clamp 210 and causing node VIN to discharge relatively slowly via resistor R2 during the vertical interval. When clamp operation resumes following the vertical interval, the desired black level at node VIN is rapidly restored.

As mentioned above, Figure 3 also shows an exemplary embodiment of reference source 220 from Figure 2 that includes

resistors R3 through R9 and MUX 360. Resistors R3 through R9 are configured as a resistor ladder that provides a plurality of reference levels having values that depend on the ratios of the resistor values. As previously discussed, specifying resistor ratios rather than particular resistor values is desirable for purposes of integrated circuit (IC) implementation.

Figure 5 shows the relationship between the reference levels generated by the arrangement in Figure 3 and an exemplary video signal waveform that would have a maximum peak-to-peak (100 IRE) amplitude of 1.9 volts. The maximum white-going amplitude shown in Figure 5 is 50 IRE which corresponds to the amplitude of an auxiliary information signal as shown in Figure 1.

Data slicer reference level VS at the output of MUX 360 is coupled to one input of comparator 230 to establish the data slicing level. As explained further below, control signals VR0 and VR1 cause MUX 360 to select one of four values (V1=15 IRE, V2=25 IRE, V3=35 IRE, V4=45 IRE) for data slicer reference level VS. MUX 360 permits the data slicing level to be adapted to the video signal amplitude as desired. Reference level VREF for black level clamp 210 is produced at the resistive mid-point (i.e. junction of resistors R7 and R8 or 125R of a total of 250R) of the resistor ladder which is equivalent to 2.5 V for VCC equal to 5 V. Sync reference level V0 is produced at the junction of resistors R8 and R9 and is coupled to one input of comparator 240 to establish the sync slicing level.

Although a sync reference level of -20 IRE would appear to be desirable for a standard sync pulse amplitude of -40 IRE, Figure 3 indicates that sync reference level V0 is approximately equal to -13.5 IRE. The indicated value of sync reference level V0 was selected because sync amplitude compression may occur in TV signals. For example, non-standard sync-to-video amplitude ratios may occur in signals extracted from video tapes. The

selected sync reference level of -13.5 IRE permits comparator 240 to accurately separate sync pulses from a video signal having sync compressed in amplitude to 1/2 of its normal value.

The voltage selection provided by MUX 360 has been configured to provide a range of slicing levels for data slicer 230 sufficient to adapt the slicing voltage to a variety of video signal variations without requiring a large MUX. Limiting the size of MUX 360 is desirable to minimize the number of control signals required and the number of devices required to implement the MUX function. For example, in an integrated circuit (IC) implementation, increasing the size of the MUX requires more transistors and more area on the IC die. In an IC, MUX 360 requires only two control signals and may be implemented using four transmission gates.

Figure 5 shows the voltages that correspond to the reference levels in Figure 3 with respect to a 1.9 volt peak-to-peak video signal. The voltage V2 input to MUX 360 provides a slicing voltage of 2.84 volts as shown in Figure 5 which is approximately equal to the 25 IRE level of a 1.9V peak-to-peak video signal. Voltage V3 at 2.98 volts is a desirable slicing level for video signals having a positive offset of 10 IRE. This type of offset may occur in video signals recorded on video tape as part of an approach to preventing unauthorized duplication of prerecorded video programs.

Two additional bias voltages, i.e. voltages V1 and V4, can be selected for optimum data slicing to adapt the slicing level to large deviations of system parameters from their nominal values. Examples of these system parameters are:

(a) video input signal amplitude different from 1.9V peak-to-peak (100 IRE white);

(b) offset voltage variations in data slicer comparator 230 (example: +/-30mV);

(c) variations in VCC for resistor ladder (example: +/-.5V);

(d) variations in resistor ratios in resistor ladder (example: +/-2%).

One of the most significant parameters affecting the slicing level is variations in the video signal amplitude. Using the exemplary variations for the parameters listed above, the maximum combined contribution of items (b), (c), (d) can be calculated to offset the slicing level by 85mV (6IRE) from the nominal value.

Various modifications of the design of reference source 220 are apparent to one skilled in the art. For example, other resistor ladder configurations may be used, and MUX'es having a different number of inputs could be selected. Thus, the described embodiment may be adapted to a variety of video signal characteristics and standards.

As described above, run-in-clock (RIC) counter 250 counts pulses of the RIC signal at the output of data slicer 230 (signal SLICED DATA in Figures 2, 3, and 4) to produce count value RIC COUNT that is indicative of when slicing reference level VS is correctly adapted to the video signal. An embodiment of counter 250 shown in Figure 4 includes counters 402, 404, and 456, D-type flip-flop (DFF) 452, NAND gates 454 and 458, and inverter 455. Count value RIC COUNT is represented by signals RIC0 and RIC1 that are produced at the two least significant outputs of counter 456 in Figure 4.

Input signals to Figure 4 include signal 128FH that serves as a clock signal for counter 402. Signal 128FH has a frequency that is 128 times horizontal frequency FH or approximately 2 MHz. Signal 128 FH may be produced at an output of a counter

associated with a phase locked loop (PLL) in the deflection circuitry of a video receiver. Signal LINE21N is generated by μC 200 in Figure 2 in response to synchronizing signal SYNC to indicate the occurrence of intervals in the video signal that are expected to include auxiliary video information, e.g. line 21 for closed caption applications. Signal LINE21N is used to reset counters 402 and 404, and may be generated by, for example, μC 200 counting line intervals as indicated by sync pulses in signal SYNC until the desired line number is located. Signals ENABLE and WR0N enable and reset, respectively, counter 456 and may be generated by μC 200. Signal WR0N resets counter 456 prior to beginning a count of RIC pulses

The timing of signals ENABLE and LINE21N is shown in Figure 6. Signal LINE21N is at logic 1 to clear (reset) counters 402 and 404 at all times except during the interval when the auxiliary video information signal is expected to occur, e.g. line 21. Signal LINE21N then goes to logic 0 to enable counters 402 and 404. Signal ENABLE is at logic 1 only during an interval of approximately 25 μs at the beginning of line 21 to enable DFF 452.

Signal RICWND at the output of DFF 452 provides an 8 μs wide window pulse that begins 12 μs after the beginning of line 21 as shown in Figure 6. The window pulse timing is selected to span an 8 μs portion of the RIC interval during line 21. The described timing of signal RICWND is generated as follows.

Both counter 404 and DFF 452 are clocked by signal CLK which is generated at the most significant output of 4-bit counter 402. Signal CLK changes every 8 cycles of the 2 MHz signal 128FH, or every 4 μs. Counters 402 and 404 are clocked by negative-going transitions (logic 1 to logic 0) in signal CLK while DFF 452 is clocked by positive-going transitions (logic 0 to logic 1) in signal CLK.

The first transition on signal CLK after counters 402 and 404 are enabled is a positive-going transition that occurs 4 μs after

signal LINE21N goes to logic 0. Although this transition clocks DFF 452, counter 404 is cleared (all outputs at logic 0) at this time because no negative-going transitions have occurred on signal CLK. As a result, a logic 0 is clocked into DFF 452 causing signal RICWND to remain at logic 0. A negative-going transition occurs on signal CLK at 8 μs after signal LINE21N goes to logic 0 causing the least significant output of counter 404 (and the D input to DFF 452) to go to logic 1. The next positive-going transition on signal CLK occurs at 12 μs after signal LINE21N goes to logic 0 causing signal RICWND to go to logic 1. At 16 μs after signal LINE21N goes to logic 0, a negative-going transition occurs on signal CLK causing the least significant output of counter 404 to go to logic 0. Thus, the next positive-going transition on signal CLK occurring at 20 μs after signal LINE21N goes to logic 0 clocks DFF 452 causing signal RICWND to go logic 0. The resulting window pulse on signal RICWND exhibits the desired 8 μs width and 12 μs delay with respect to the beginning of line 21 as shown in Figure 6.

Counter 456 is enabled via NAND gate 454 for counting RIC pulses on signal SLICED DATA when signals WR0N and RICWND are at logic 1, i.e. during the window pulse when counter 456 is not being reset. Counter 456 is disabled when a count of 3 (RIC0=RIC1=logic 1) is reached via NAND gate 458. A count of 3 indicates that the RIC signal is being sliced correctly. This feature prevents 4-bit counter 456 from "wrapping around" to a count of 0 after a count of 3 has been reached, thereby preventing a potential spurious count of 0 when the RIC signal is actually present and is being sliced correctly. Thus, a count of 3 actually indicates at least 3 pulses have occurred on signal SLICED DATA.

Modifications of the arrangement in Figure 4 are possible. For example, 4-bit counters have been used for counters 404 and 456 because 4-bit counters are typical digital "building blocks". However, other devices may be used. Counter 404 could be replaced with a toggle flip-flop that is clocked by signal CLK.

Counter 456 could be a 2-bit counter. In addition, count values other than 3, e.g. 2, 4 or 5, could be used to indicate the correct slicing of the RIC signal because 7 cycles of the RIC signal occur during the RIC interval. However, a value of 3 provides a degree of noise immunity in comparison to using a count of 2 while requiring fewer counter stages (only 2) than are needed for a count of 4 or 5 (3 counter stages). Also, it may be possible to eliminate counters 402 and 404 if another source of signal CLK and the input signal for DFF 452 exists in the video signal processing system. For example, the system may include an on screen display (OSD) feature that includes one or more counters for providing various signals at frequencies that are multiples of the horizontal line frequency FH.

Signals RIC0 and RIC1 in Figure 4 are tested by μC 200 after the end of the 8 μs window interval to determine the count value. For the exemplary embodiment shown in Figures 2, 3, and 4, counting of the RIC signal pulses occurs when transitions of signal SLICED DATA clock counter 456. Thus, a count value of 0 (RIC0=RIC1=logic 0) results if no transitions occur, e.g. if data slicing reference level VS always exceeds the maximum RIC pulse amplitude. Similarly, a count value of 1 (RIC0=logic 1 and RIC1=logic 0) occurs when a single transition occurs on signal SLICED DATA. For example, when the slicing level is always less than the minimum value of the RIC waveform pulses, only one transition from the blanking level to the beginning of the RIC waveform occurs.

If the slicing level is set to a point between these two extreme values, the sensitivity of the disclosed system is such that deviations of the slicing level from the ideal slicing level (mid-point of the peak-to-peak range of the RIC signal) will not prevent the counter from being clocked to a count of 3. Experimental results have indicated that when a count of 3 is being generated, the system accurately extracts auxiliary video data. Thus, counts

of 0 (slicing level too high), 1 (slicing level too low), or 3 (slicing level acceptable) can be expected as depicted in the waveforms for signal SLICED DATA that are shown in Figures 6A, 6C, and 6B, respectively.

In regard to Figures 6A and 6B, the RIC waveform shown exhibits spikes at the tips of the RIC waveform that extend beyond the slicing level. It would appear that these spikes might be sufficient to clock counter 456 such that RIC COUNT would not be 0 and 1 as shown in Figures 6A and 6C, respectively. However, signal SLICED DATA as shown in Figure 6 was generated from signal VIDEO as shown in Figure 6 using an alternative embodiment of the arrangement in Figure 2. This alternative embodiment includes filtering features that are described further below and are shown in Figures 11 and 12. Briefly, the filtering removes the described spikes prior to counter 250 and low pass filters the video signal prior to data slicing. As shown in Figure 6, the low pass filter reduces the amplitude of the RIC signal amplitude to a value that is less than the nominal 50 IRE amplitude shown in Figures 1 and 5.

As long as counts of 3 are being produced, there is no need to modify the slicing level. If μC 200 detects a count of 0, the slicing level may be decreased by μC 200 selecting a different value for signal VR in Figure 2 (control signals VR0 and VR1 for MUX 360 in Figure 3). For example, referring to Figure 3, if the current value of slicing reference voltage VS is voltage V2, μC 200 could respond to a count of 0 by changing control signal VR to select voltage V1. Similarly, μC 200 could increase the slicing reference voltage in response to a count of 1 by changing control signal VR to select voltage V3 or V4. Thus, the slicing level can be modified rapidly in response to count values other than 3.

The described features provide data slicing level adjustment apparatus that rapidly adapts the slicing level to the video signal level. More specifically, the system can respond to changes in

video signal levels during each video frame interval because the slicing level may be tested after each occurrence of line 21 in field 1. In addition, slicing level adjustment can operate continuously in the background under control of µC 200. Under certain conditions, however, it is desirable for the slicing level to be held constant despite changes in the video signal level. For example, the slicing level should remain constant during brief transients or signal "dropouts" to provide consistent data extraction when the normal signal level resumes.

The disclosed apparatus addresses conditions such as dropout by providing for monitoring the number of times that the various counts of 0, 1, and 3 occur. For example, if RIC COUNT is usually equal to 3 and a count of 0 or 1 occurs infrequently, it is likely that the slicing level is correct and that the occasional counts of 0 or 1 are being caused by effects such as signal dropout. Thus, no change in the slicing level is needed. If counts of 0 occur frequently, the slicing level is adjusted to a lower value while frequent counts of 1 cause the slicing level to be adjusted to a higher value.

The monitoring of the frequency of occurrence of particular count values could be accomplished by, for example, µC 200 executing a procedure that increments and decrements values stored in registers internal to µC 200. As an example, consider the flowchart shown in Figure 7 that depicts the described monitoring operation of µC 200 using two registers designated RICCNT0 and RICCNT3 in the context of closed caption information. Register RICCNT0 serves as a "flag" that is set to indicate the occurrence of a count of 0. Register RICCNT3 is a multi-bit register having a value that is incremented and decremented as described below.

In Figure 7, after initializing the registers, a new value of RIC COUNT is generated and tested. If RIC COUNT equals 3, the system presumes that a valid slicing level may exist. As a result, register RICCNT0 is cleared and the value in register RICCNT3 is

incremented if that value is less than a limit value, e.g. 16. Note that limit values other than 16, e.g. 7, may be used to reduce the number of register bits required to store the value of RICCNT3. When RIC COUNT is 0 rather than 3, RICCNT0 is set and RICCNT3 is decremented. After decrementing, the value of RICCNT3 is tested. RICCNT3 equal to 0 indicates that RIC COUNT has not been 3 for a number of tests equal to the limit value (16 in Figure 7) indicating that an adjustment of the slicing level is needed. If register RICCNT0 is set at this time, the value of RIC COUNT was 0 indicating that the slicing level should be increased. Register RICCNT0 being reset indicates that RIC COUNT was 1 (not 3 and not 0). As a result, the slicing level should be decreased.

Thus, the slicing level will not be adjusted until register RICCNT3 has a value of 0. As a result, the slicing level will be adjusted only after a delay has elapsed following the change of RIC COUNT from a value of three to a value that is not 3. For example, if RICCNT3 is 5, RIC COUNT has had a value of 3 for the previous 5 tests and the slicing level will not be adjusted unless the next 5 consecutive tests of RIC COUNT produce values other than 3. In this case, a delay of 5 test intervals is introduced before the slicing level is adjusted. The maximum delay is equal to the limit value for RICCNT3, e.g. 16 test intervals in Figure 7. Figure 8 shows a listing of a software program for a Motorola MC68HC05 processor corresponding to the flowchart in Figure 7.

The approach illustrated in Figure 7 adjusts the slicing level rapidly when necessary because the program either increases of decreases the slicing level as needed. As described above, this is accomplished by changing the value of control signals VR0 and VR1 for MUX 360 in Figure 3. Control signals VR0 and VR1 may be generated at the outputs of a 2-bit counter. For example, incrementing the counter could produce a new value for signals VR0 and VR1 that would select a higher value for slicing reference

level VS. Decrementing the counter would then select a lower slicing level.

For the exemplary embodiment shown in Figure 3 where the number of possible reference levels is small, it may be unnecessary to include the capability to determine whether the slicing level should be increased or decreased. For example, if a 2-bit counter is used to generate signals VR0 and VR1, the counter could count in one direction only and select all possible reference levels if the counter is designed to wrap around. This approach is depicted in the flowchart shown in Figure 9.

In Figure 9, the only adjustment to the slicing level is to "increase" the slicing level. When the maximum slicing level is reached, e.g. voltage V4 in Figure 3, the next "increase" will actually result in selecting the minimum slicing voltage, e.g. voltage V1 in Figure 3. Thus, the voltage selection wraps around as described in the preceding paragraph. The approach illustrated in Figure 9 may be slightly slower to reach an acceptable slicing level than the approach in Figure 7 if the selection procedure must sequence through all possible slicing level values. However, implementing the approach of Figure 9 in software requires fewer instructions as is apparent when comparing the exemplary program listing in Figure 10 that corresponds to the flowchart in Figure 9 to the program listing in Figure 8.

As mentioned above, Figures 11 and 12 show an alternative embodiment for the apparatus in Figure 2. The arrangement in Figure 11 differs from that in Figure 2 in that low-pass filter 1160 and spike filter 1170 are included. Features 200 through 250 in Figure 11 correspond to features in Figure 2 that are numbered the same.

Low-pass filter 1160 may be implemented using a single-pole RC-type low pass filter such as that shown in Figure 12A. The circuit shown in Figure 12A has a pole at 700KHz and reduces the amplitude of the 500KHz run-in clock sinewave by about 80

percent from the nominal 50 IRE value (see Figures 1 and 5) as can be seen in Figure 6. The reduction in the amplitude of the run-in clock relative to that of the data signal is advantageous because the range of RIC values is decreased correspondingly decreasing the adjustment range necessary for the slicing level.

Spike filter 1170 is inserted into the signal path at the output of data slicer 230. Spike filter 1170 improves the accuracy with which the slicing level is set because, similarly to the action of the low-pass filter, the amplitude range of the RIC signal is decreased by eliminating the spike peaks on the RIC portion of the video waveform as shown in Figure 6. A digital embodiment of the spike filter is shown in Figure 12B. The circuit in Figure 12B eliminates from the data slicer output all pulses narrower than 280ns and passes all pulses wider than 420ns. As a result, with the slicer bias at a value near the positive or negative tips of the run-in clock in the video input, the resulting output pulses of the data slicer are eliminated by the spike filter if they are sufficiently narrow. The effect of the spike filter is demonstrated by the waveforms shown in Figure 6.

CLAIMS

1. Apparatus for processing a video signal including horizontal synchronizing pulses indicating the start of respective horizontal line intervals, and including an auxiliary information component occurring during at least one of said horizontal line intervals, said auxiliary information component including a reference component and a data component, said apparatus comprising:

means having an input coupled to said video signal for producing an output signal having one of first and second values, said output signal having said first value when said video signal exceeds a threshold level and said output signal having said second value when said video signal is less than said threshold level;

means for generating said threshold level and for modifying said threshold level in response to a control signal; and

control means for detecting occurrence of said reference component in said output signal, for determining if said horizontal line intervals during which said reference component is detected occur at a predetermined rate, and for generating said control signal to modify said threshold level if said horizontal line intervals during which said reference component is detected do not occur at said predetermined rate.

2. The apparatus of claim 1, wherein said control means comprises means for generating a count value in response to detection of said reference component;

said count value being modified in a first direction when said reference component is detected during one of said horizontal line intervals expected to include said auxiliary information component;

said count value being modified in a second direction opposite to said first direction when said reference component is not detected during one of said horizontal line intervals expected to include said auxiliary information component; and

said control means generating said control signal to modify said threshold level when said count value is not a predetermined value.

3. The apparatus of claim 1, wherein said reference component exhibits periodic amplitude variations during a particular interval within each of said horizontal line intervals that include said auxiliary information component, and said control means comprises:

means for counting in response to amplitude variations in said output signal during a portion of said particular interval within each of said horizontal line intervals expected to include said auxiliary information component to produce a count value representative of the number said periodic amplitude variations of said reference component that occur during said portion of said particular interval, detection of said reference component being indicated when said count value is at least a predetermined value.

4. The apparatus of claim 1, wherein said reference component exhibits periodic amplitude variations during a particular interval within each of said horizontal line intervals that include said auxiliary information component, and said control means comprises:

means for counting in response to amplitude variations in said output signal during a portion of said particular interval within each of said horizontal line intervals expected to include said auxiliary information component to produce a first count value representative of the number said periodic amplitude variations of said reference component that occur during said portion of said particular interval, detection of said reference component being indicated when said count value is at least a predetermined value;

said counting means generating a second count value in response to said first count value indicating detection of said reference component;

said second count value being modified in a first direction when said reference component is detected during one of said horizontal line intervals expected to include said auxiliary information component;

said second count value being modified in a second direction opposite to said first direction when said reference component is not detected during one of said horizontal line intervals expected to include said auxiliary information component; and

said control means generating said control signal to modify said threshold level when said second count value is not a predetermined value.

5. The apparatus of claim 4 wherein said control signal from said control means comprises a digital signal representative of a desired threshold level and said threshold level modifying means comprises a digital to analog converter responsive to said digital signal for producing said threshold level.

6. The apparatus of claim 3 further comprising filter means in said video signal path for substantially preventing amplitude variations in said video signal other than said periodic variations of said reference component from affecting said count value produced by said counting means.

7. The apparatus of claim 6 wherein said filter means comprises a low pass filter coupling said video signal to said input of said output signal producing means and a spike filter coupling said output signal to said control means.

8. The apparatus of claim 7 wherein said spike filter is a digital filter.

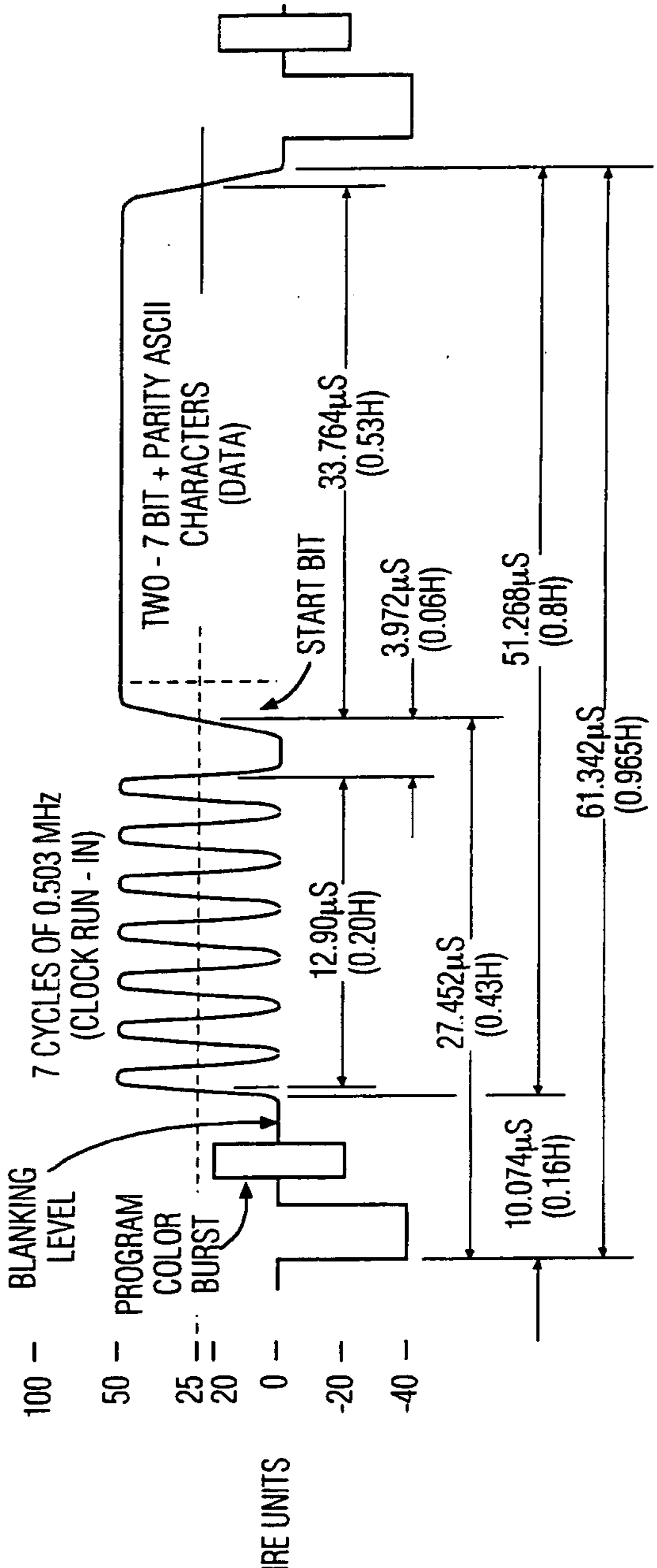


FIG. 1

SUBSTITUTE SHEET

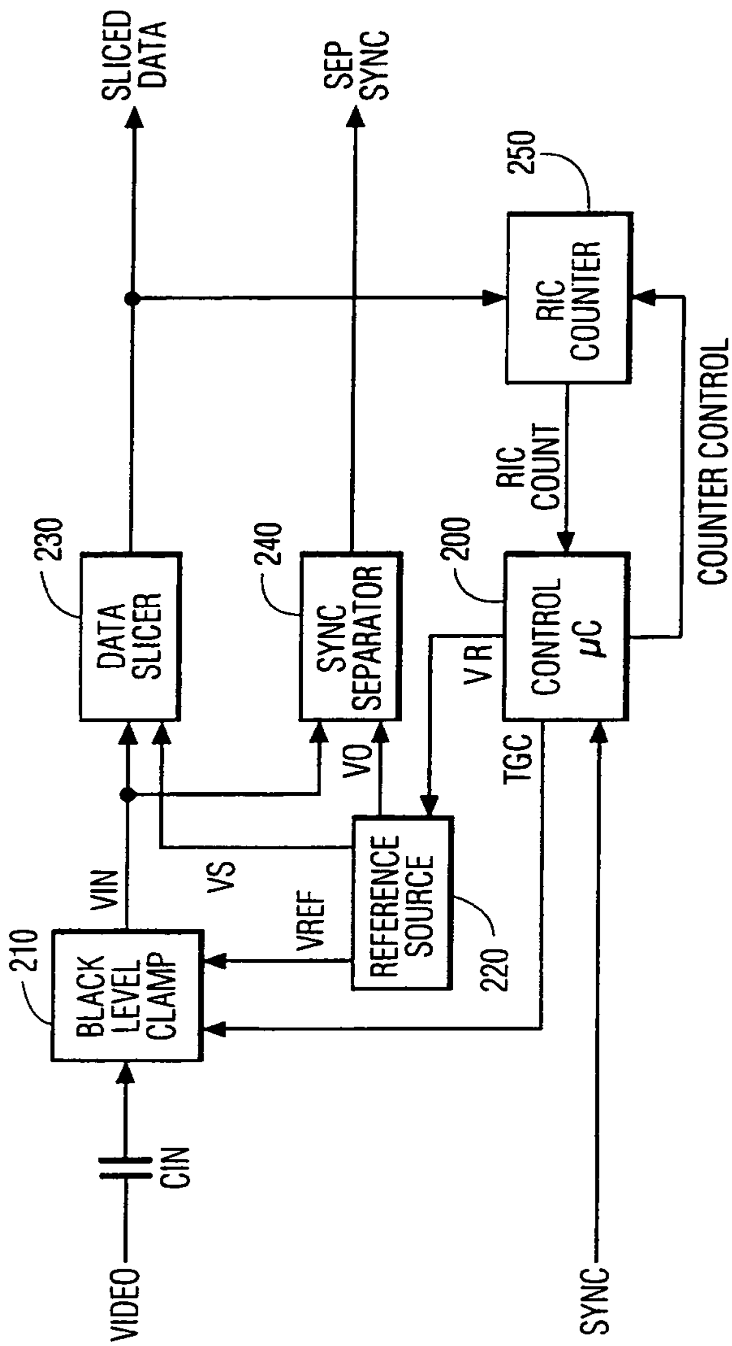

SLICED DATA
SEP SYNC
250
RIC COUNTER
RIC COUNT
COUNTER CONTROL
230
DATA SLICER
240
SYNC SEPARATOR
200
CONTROL μC
V R
TGC
VO
VS
VIN
VREF
REFERENCE SOURCE
220
210
BLACK LEVEL CLAMP
CIN
VIDEO
SYNC

FIG. 2

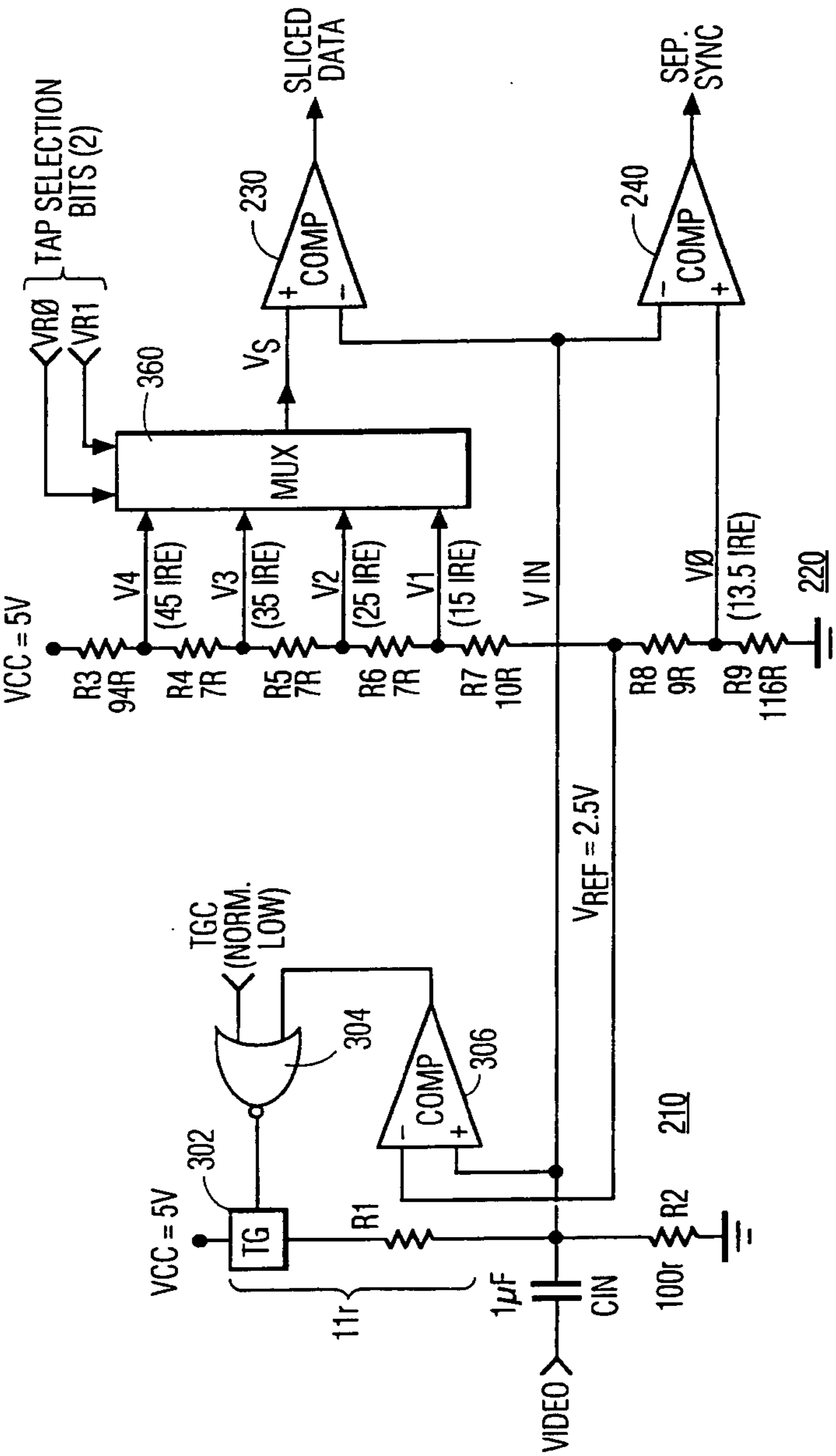

TAP SELECTION BITS (2)
VRØ
VR1
SLICED DATA
SEP. SYNC
230
COMP
240
COMP
360
MUX
V_S
VCC = 5V
R3 94R
R4 7R
R5 7R
R6 7R
R7 10R
R8 9R
R9 116R
V4 (45 IRE)
V3 (35 IRE)
V2 (25 IRE)
V1 (15 IRE)
V IN
VØ (13.5 IRE)
220
V_{REF} = 2.5V
TGC (NORM. LOW)
304
306
COMP
302
TG
R1
R2
11r
1µF
CIN
100r
210
VIDEO

FIG. 3

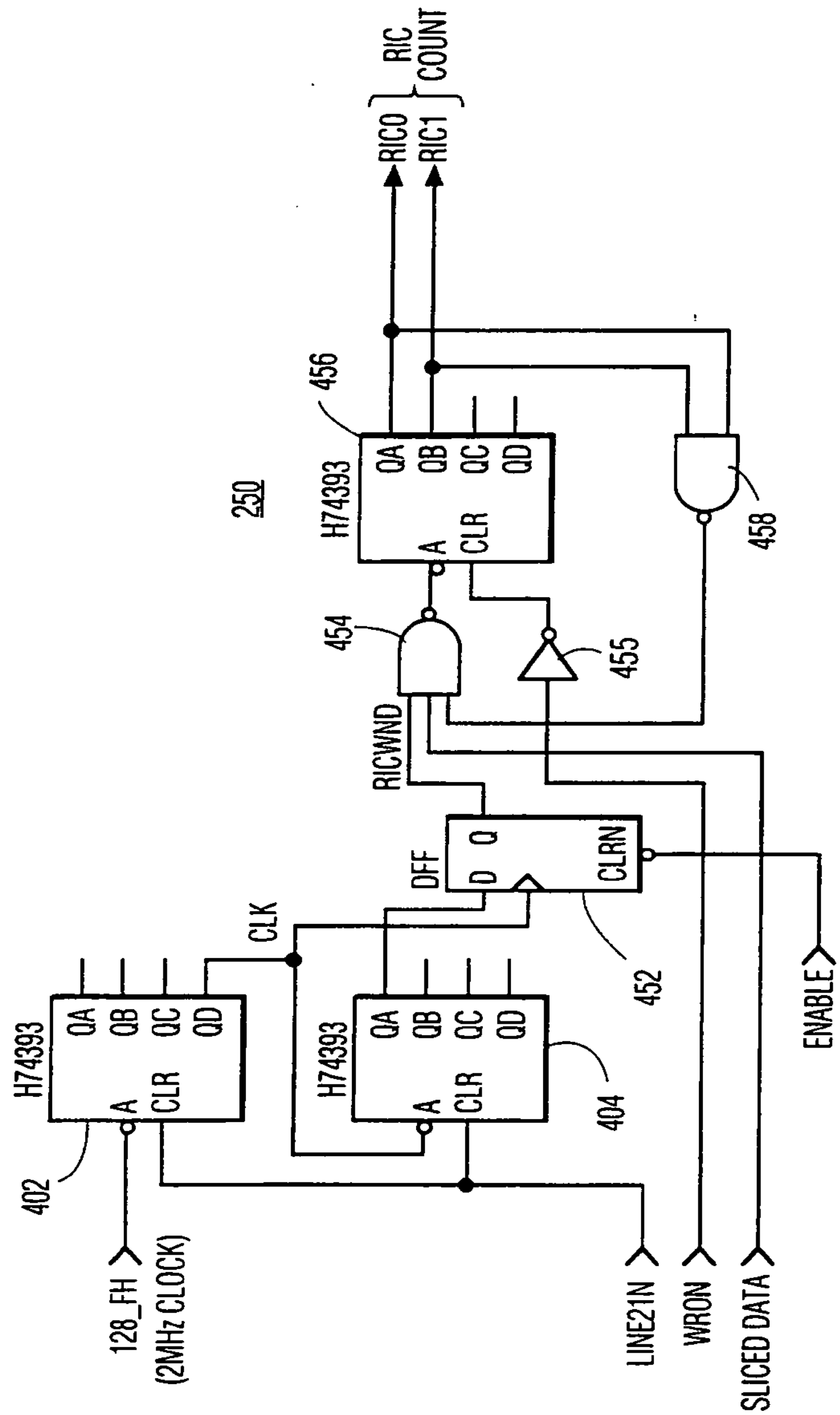
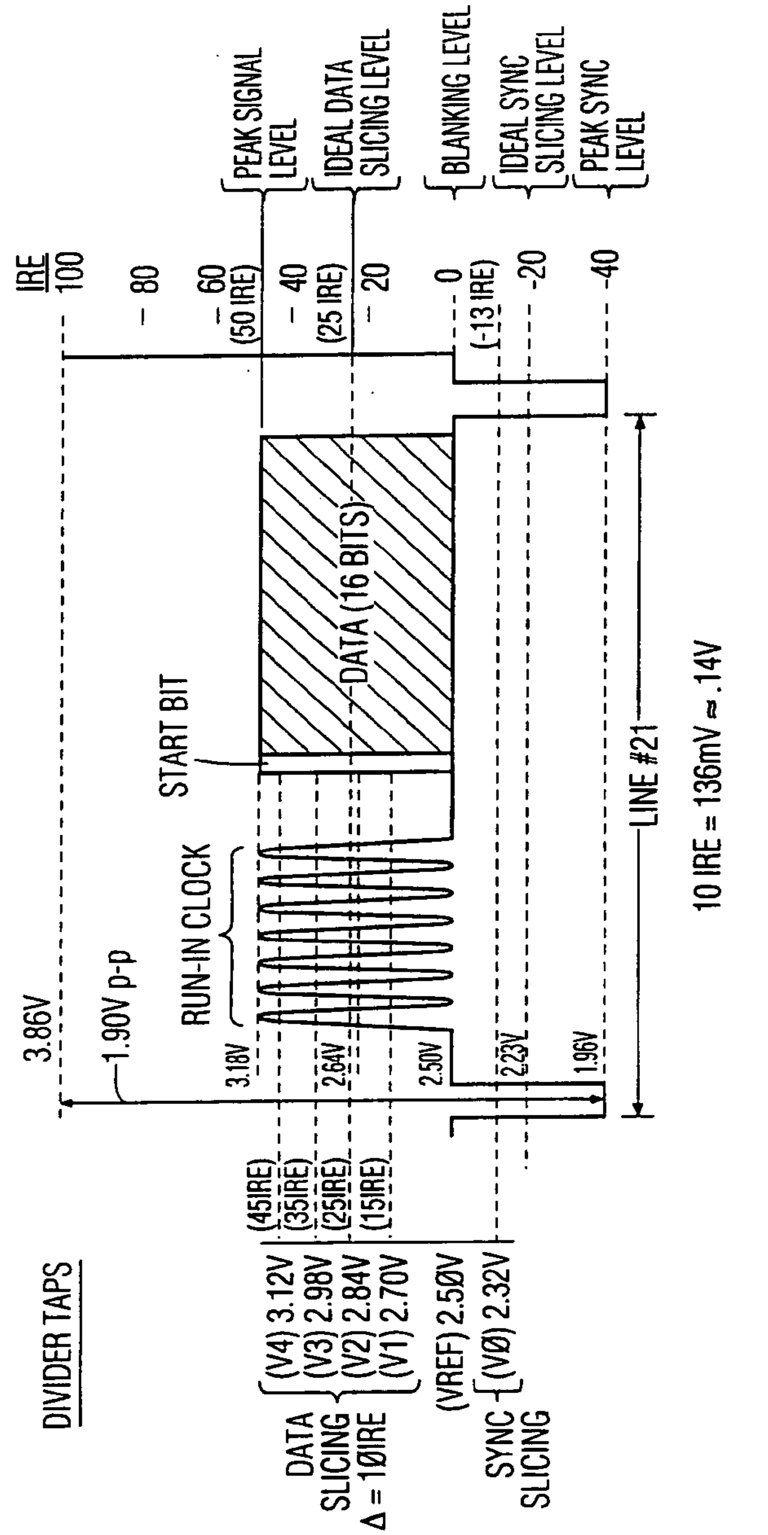
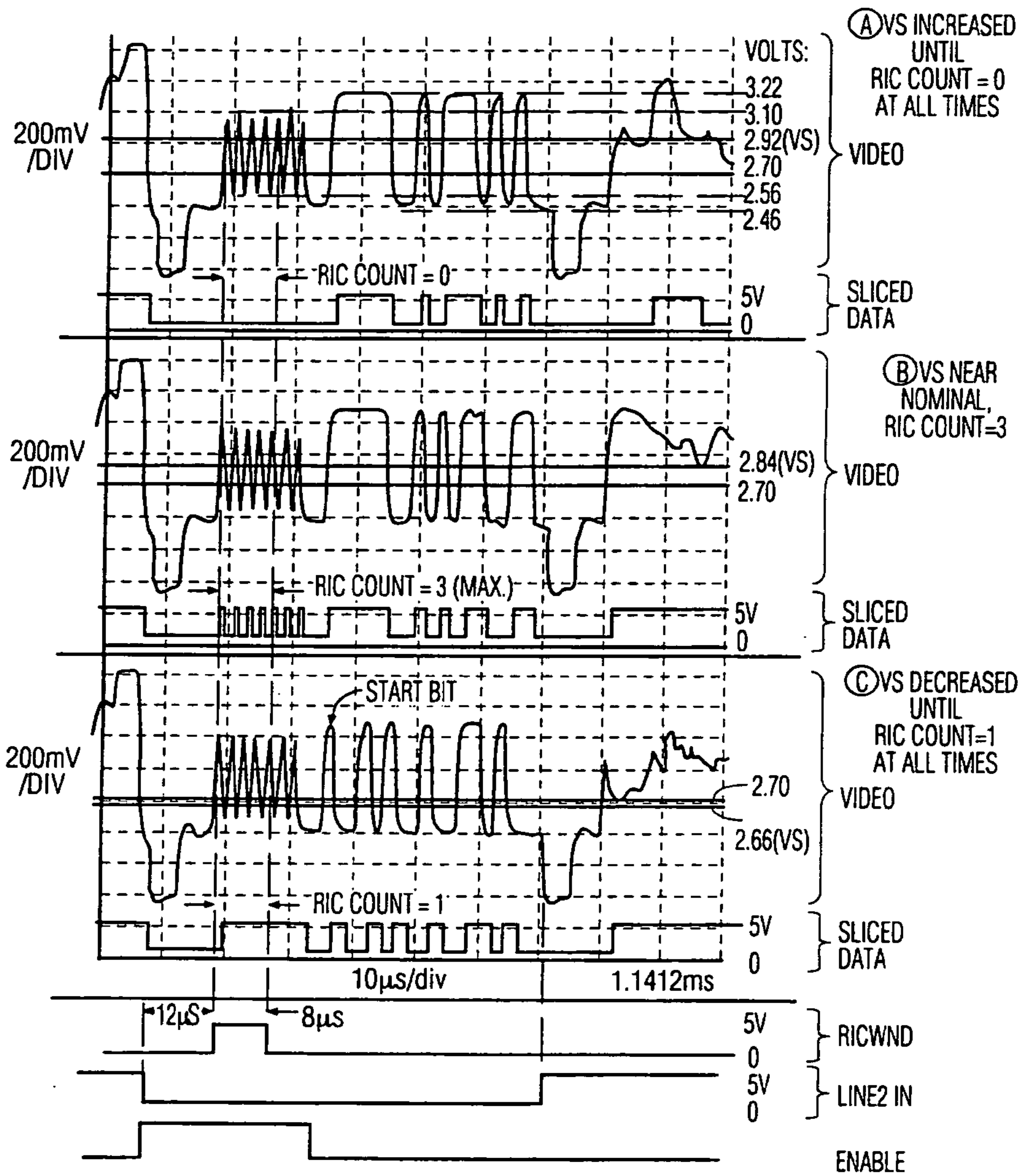

RIC0
RIC1
RIC COUNT
250
456
H74393
QA
QB
QC
QD
A
CLR
458
454
455
RICWND
DFF
D
Q
CLRN
CLK
452
ENABLE
H74393
QA
QB
QC
QD
A
CLR
402
H74393
QA
QB
QC
QD
A
CLR
404
128_FH
(2MHz CLOCK)
LINE21N
WRON
SLICED DATA

FIG. 4



PEAK SIGNAL LEVEL
IDEAL DATA SLICING LEVEL
BLANKING LEVEL
IDEAL SYNC SLICING LEVEL
PEAK SYNC LEVEL
IRE
100
80
60
(50 IRE)
40
(25 IRE)
20
0
(-13 IRE)
-20
-40
START BIT
DATA (16 BITS)
RUN-IN CLOCK
3.86V
1.90V p-p
3.18V
2.64V
2.50V
2.23V
1.96V
LINE #21
10 IRE = 136mV ≈ .14V
DIVIDER TAPS
DATA SLICING Δ = 1ØIRE
(V4) 3.12V (45IRE)
(V3) 2.98V (35IRE)
(V2) 2.84V (25IRE)
(V1) 2.70V (15IRE)
(VREF) 2.5ØV
SYNC SLICING (VØ) 2.32V

FIG. 5



VOLTS:
3.22
3.10
2.92(VS)
2.70
2.56
2.46
200mV /DIV
Ⓐ VS INCREASED UNTIL RIC COUNT = 0 AT ALL TIMES
VIDEO
RIC COUNT = 0
5V
0
SLICED DATA
Ⓑ VS NEAR NOMINAL, RIC COUNT=3
2.84(VS)
2.70
VIDEO
RIC COUNT = 3 (MAX.)
SLICED DATA
Ⓒ VS DECREASED UNTIL RIC COUNT=1 AT ALL TIMES
START BIT
2.70
2.66(VS)
VIDEO
RIC COUNT = 1
SLICED DATA
10μs/div
1.1412ms
12μS
8μs
RICWND
LINE2 IN
ENABLE

FIG. 6

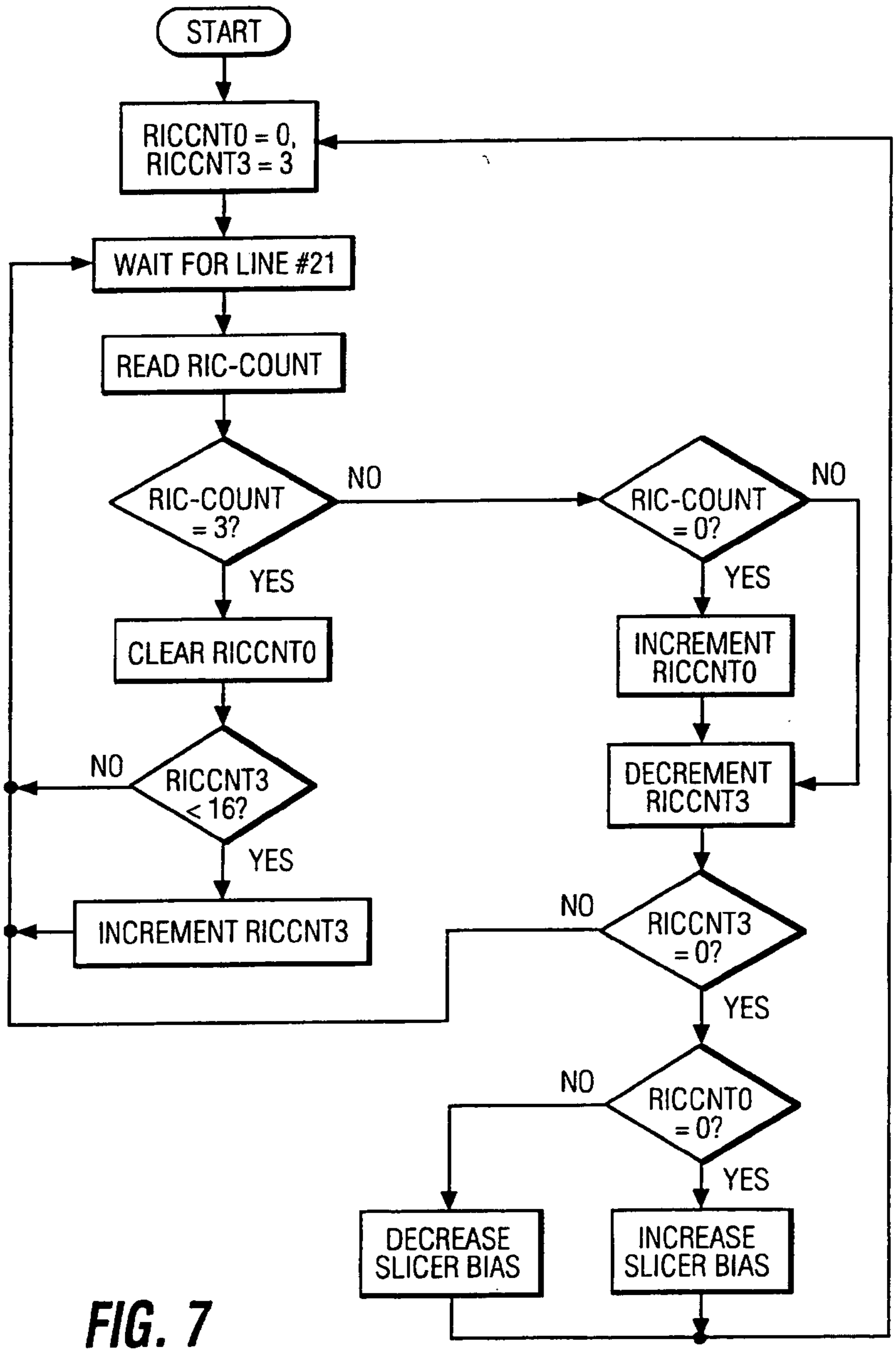

START
RICCNT0 = 0,
RICCNT3 = 3
WAIT FOR LINE #21
READ RIC-COUNT
RIC-COUNT = 3?
NO
YES
CLEAR RICCNT0
RICCNT3 < 16?
NO
YES
INCREMENT RICCNT3
RIC-COUNT = 0?
NO
YES
INCREMENT RICCNT0
DECREMENT RICCNT3
RICCNT3 = 0?
NO
YES
RICCNT0 = 0?
NO
YES
DECREASE SLICER BIAS
INCREASE SLICER BIAS

FIG. 7

```
214  214A  0E 58 0E  DSBALG    BRSET  7, STSCODE, DSBMODE
215  214D  3C 5E               INC    IDLECNT              ; IF START BIT HAS NOT DETECTED IN THE LAST
216  214F  B6 5E               LDA    IDLECNT              ;   20 FRAMES, REINITIALIZE
217  2151  A1 14               CMP    #20
218  2153  25 03               BLO    ALGX
219  2155  CC 20 1F            JMP    INPROCA
221  215B  3F 5E     DSBMODE   CLR    IDLECNT
222  215D  0A 00 3C            BRSET  5, PORT$A, MFMODE    ; IF BIT5/A=0, EXECUTE STEP 224
223
224  2160  B6 58               LDA    STSCODE              ; CHECK WHETHER RIC-COUNT IS 3
225  2162  A4 03               AND    #$03
226  2164  A1 03               CMP    #$03
227  2166  26 0C               BNE    LP1
228  2168  3F 5B               CLR    RICCNT0              ; IF YES, CLEAR RIC-COUNT=0 COUNTER AND
229  216A  B6 5D               LDA    RICCNT3              ;   INCREMENT RIC-COUNT=3 COUNTER UP TO 16
230  216C  A1 10               CMP    #16                  ;   BEFORE EXITING
231  216E  24 23               BHS    LPNX
232  2170  3C 5D               INC    RICCNT3
233  2172  20 25               BRA    LPNX
234  2174  A1 00     LP1       CMP    #$00                 ; IF RIC-COUNT IS 0, INCREMENT RIC-COUNT =0
235  2176  26 02               BNE    LP2
236  2178  3C 5B               INC    RICCNT0
237  217A  3A 5D     LP2       DEC    RICCNT3              ; DECREMENT RIC-COUNT=3 COUNTER FOR RIC-COUNT5
238  217C  26 1B               BNE    LPNX                 ;   OF 0, 1, OR 2 AND EXIT IF CONTENTS > 0
239  217E  3D 5B               TST    RICCNT0              ; IF COUNT IN RICCNT3 IS DOWN TO 0, DECIDE
240  2180  27 0A               BEQ    LP3                  ;   IF RICCNT0 > 0, DECREASE BIAS BY ONE STEP
241  2182  B6 57               LDA    DSCODE               ;   (DO NOT ALLOW WRAP-AROUND!)
242  2184  A1 40               CMP    #$40
243  2186  25 0E               BLO    LPX
244  2188  A0 40               SUB    #$40
245  218A  20 08               BRA    LP4
246  218C  B6 57     LP3       LDA    DSCODE               ;   IF RIICCNT=0, INCREASE BIAS BY ONE STEP
247  218E  A1 C0               CMP    #$C0                 ;   (DO NOT ALLOW WRAP-AROUND!)
248  2190  24 04               BHS    LPX
249  2192  AB 40               ADD    #$40
250  2194  B7 57     LP4       STA    DSCODE
251  2196  CC 20 26  LPX       JMP    INPROCB
252  2199  CC 20 2C  LPNX      JMP    BEGPROC
```

FIG. 8.

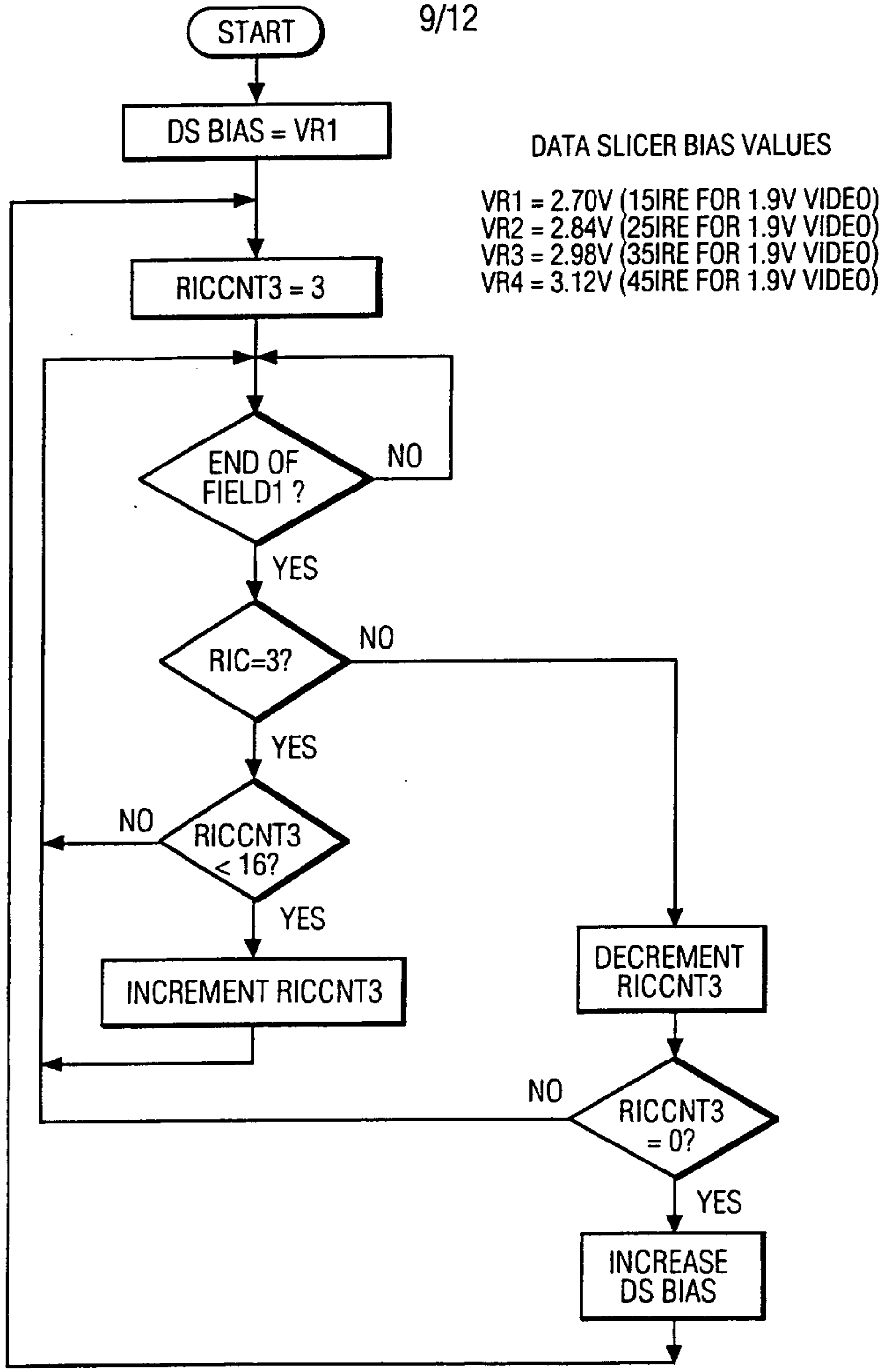

START
DS BIAS = VR1
DATA SLICER BIAS VALUES
VR1 = 2.70V (15IRE FOR 1.9V VIDEO)
VR2 = 2.84V (25IRE FOR 1.9V VIDEO)
VR3 = 2.98V (35IRE FOR 1.9V VIDEO)
VR4 = 3.12V (45IRE FOR 1.9V VIDEO)
RICCNT3 = 3
END OF FIELD1 ?
NO
YES
RIC=3?
NO
YES
RICCNT3 < 16?
NO
YES
INCREMENT RICCNT3
DECREMENT RICCNT3
RICCNT3 = 0?
NO
YES
INCREASE DS BIAS

FIG. 9

```
                    ; -------------------AUTOMATIC BIAS ADJUSTMENT ROUTINE-------------------
2098  B6  58              LDA   STSCODE      ; CHECK WHETHER RIC-COUNT IS 3
209A  A4  03              AND   #$03
209C  A1  03              CMP   #$03
209E  26  0A              BNE   LP1
20A0  B6  68              LDA   RICCNT3      ; IF YES, INCREMENT RICCNT3 UP TO 7
20A2  A1  07              CMP   #7
20A4  24  12              BHS   LPX
20A6  3C  68              INC   RICCNT3
20A8  20  0E              BRA   LPX
20AA  3A  68        LP1   DEC   RICCNT3      ; ELSE, DECREMENT RICCNT3 AND CHECK FOR 0
20AC  26  0A              BNE   LPX
20AE  B6  55              LDA   DSCODE       ; IF RICCNT3=0, INCREASE BIAS BY ONE STEP
20B0  AB  40              ADD   #$40         ;   (WRAP-AROUND IS PERMITTED)
20B2  B7  55              STA   DSCODE
20B4  A6  03              LDA   #3
20B6  B7  68              STA   RICCNT3
20B8  20  0E        LPX   BRA   MONWRT       ; EXIT BIAS ADJUSTMENT ROUTINE
```

FIG. 10

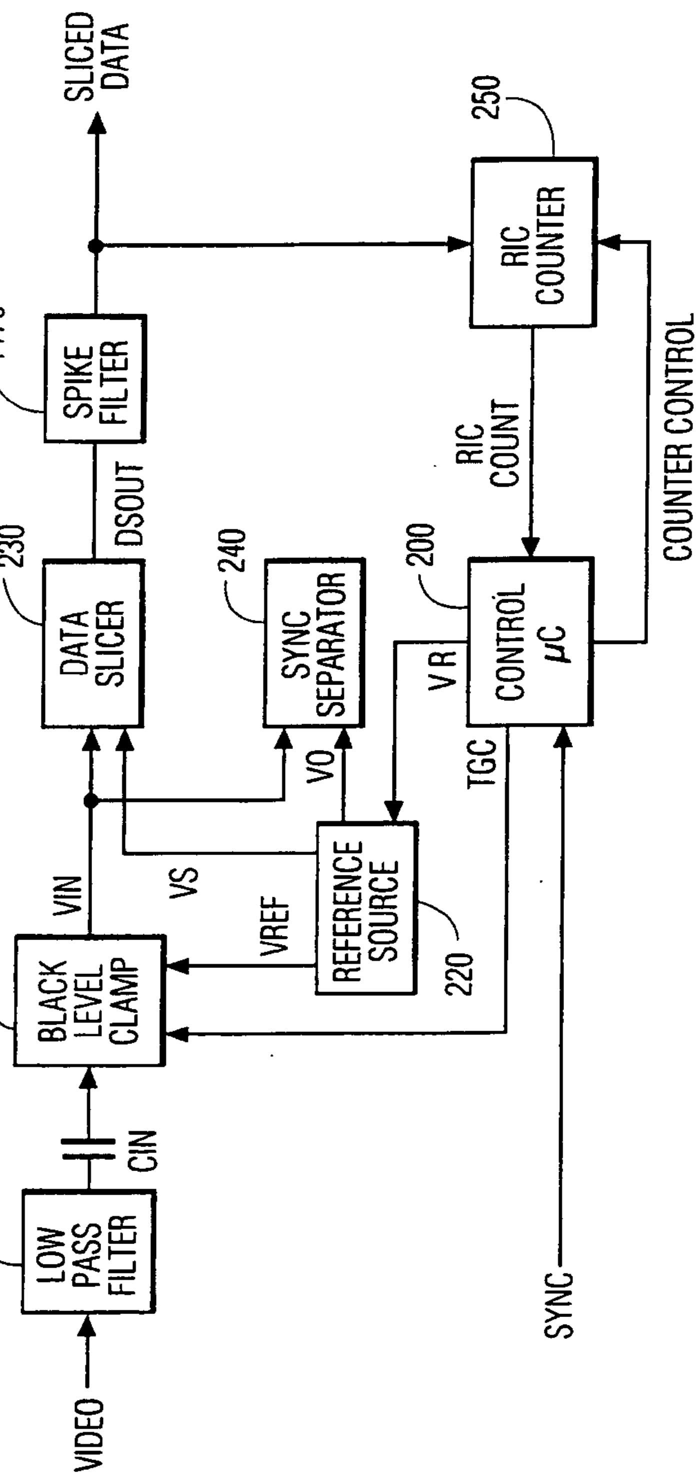

VIDEO
LOW PASS FILTER
1160
CIN
BLACK LEVEL CLAMP
210
VIN
VS
VREF
REFERENCE SOURCE
220
DATA SLICER
230
DSOUT
SYNC SEPARATOR
240
VO
SPIKE FILTER
1170
SLICED DATA
RIC COUNTER
250
RIC COUNT
COUNTER CONTROL
CONTROL μC
200
V R
TGC
SYNC

FIG. 11

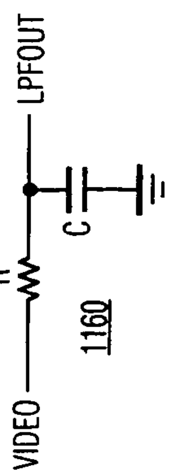


FIG. 12A

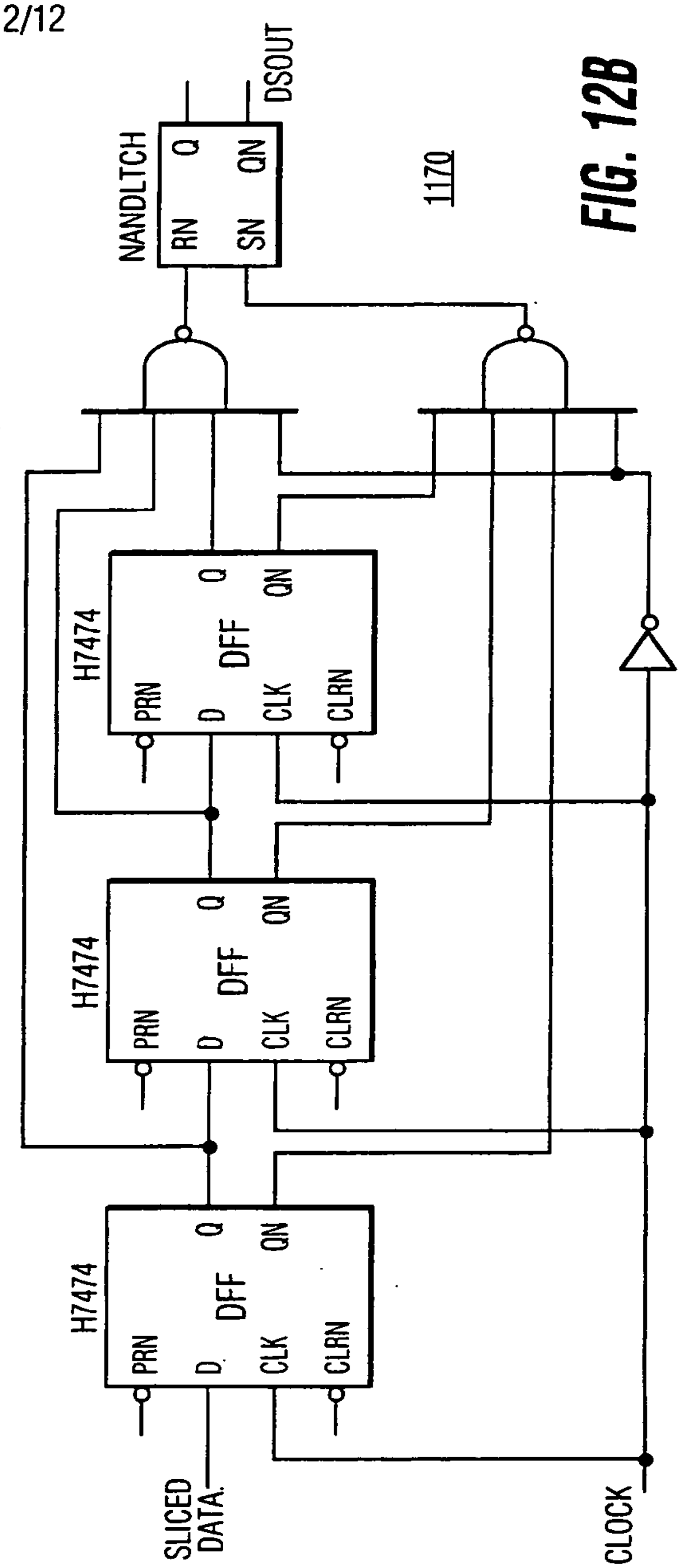


FIG. 12B

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 93/07163

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H04N7/087

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 421 897 (SGS-THOMSON MICROELECTRONICS S. A.) 10 April 1991 see column 4, line 23 - column 5, line 47 see column 6, line 25 - column 7, line 7; figures 1-6 ---	1-8
A	IEEE TRANSACTIONS ON CONSUMER ELECTRONICS vol. 36, no. 3 , August 1990 , NEW YORK US pages 693 - 698 XP162908 J. MEYER 'TELETEXT: A True Monochip Solution.' see page 695, column 1, line 1 - line 29; figures 4A,4B ---	6-8
A	PATENT ABSTRACTS OF JAPAN vol. 10, no. 201 (E-419)15 July 1986 & JP,A,61 043 886 (HITACHI) 3 March 1986 see abstract -----	1-5

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
21 December 1993	21. 01. 94

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+ 31-70) 340-3016	Verleye, J

INTERNATIONAL SEARCH REPORT

Information on patent family members

Interna. . l Application No
PCT/US 93/07163

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-0421897	10-04-91	FR-A- 2652697	05-04-91
		JP-A- 3127576	30-05-91
		US-A- 5136382	04-08-92

Form PCT/ISA/210 (patent family annex) (July 1992)